REMARKS

Reconsideration and allowance of the present application are respectfully requested. Claims 1-9 remain pending in the application. By this Amendment, claim 1 is amended.

In numbered paragraph 1, independent claim 1, along with various dependent claims, is rejected as being unpatentable over U.S. Patent 6,609,167 (Bastiani et al.) in view of US Patent 6,718,413 (Wilson et al.). In numbered paragraph 2, dependent claim 9 is rejected as being unpatentable over the Bastiani et al. patent, in view of the Wilson et al. patent and U.S. Patent 5,555,430 (Gephardt et al.). These rejections are respectfully traversed.

Applicants have disclosed a transceiver configured for use with a multi-tier system bus that allows for the flow of information to be managed among plural processors by connecting processors within modules on a local bus, which is then connected to the system bus by way of a gateway. The transceiver can be used for interconnecting plural processors in a bus environment (e.g., specification at paragraph [0001]). The plural processors can be connected using the bus system to function as a processor array (e.g., specification at paragraph [0005]). As exemplified in Fig. 1, a system bus 104 controls and arbitrates access to the system bus 102 (paragraph [0013]). As exemplified in Fig. 2, a transmitter portion provides buffering and interleaved output of direct memory access and control actions packet types. A receiver portion provides input discrimination and individual buffering of direct memory access and interrupt control actions packets along with specialized control functions, e.g., reset, timer, broadcast, etc.

The foregoing features are broadly encompassed by claim 1, which recites, among other features, a transceiver for use within a multi-tier system bus configuration, including means for independently receiving instructions via the system bus from at least one of a plurality of processors, means for independently transmitting instructions via the system bus to at least one of the plurality of processors, means for buffering instructions received via the system bus, and means for buffering instructions transmitted via the system bus, wherein access to the multi-tier system bus is arbitrated.

The Bastiani et al. patent does not teach or suggest a plurality of processors accessing a system bus that is arbitrated. In paragraph 1, page 3 of the final Office Action, the Examiner admits that "Bastiani does not explicitly teach wherein access to the multi-tier system bus is arbitrated."

The Wilson et al. patent does not cure the deficiencies of the Bastiani et al. patent. The Wilson et al. patent discloses contention-based methods for generating reduced number of interrupts between a host computer 302 and SCSI device 306 through a host bus 314 (col. 5, lines 54-64). The Wilson et al. patent does not teach or suggest a plurality of processors accessing a system bus that is arbitrated.

The Gephardt et al. patent does not cure the deficiencies of the Bastiani et al. patent and the Wilson et al. patent. The Gephardt et al. patent was applied for its disclosure of interrupt management in a multiprocessing system (col. 22, line 61 through col. 23, line 17). However, the Gephardt et al. patent does not teach or suggest the recited features of claim 1. Claim 9 depends from claim 1. Accordingly, at least for these reasons, claim 9 is allowable.

There is no motivation to combine the Bastiaini et al. patent, the Wilson et al. patent and/or the Gephardt et al. patent. The Bastiani et al. patent discloses a serial communication between a host computer 102 and one or more serial protocol devices. The Wilson et al. patent discloses contention-based methods for generating reduced number of interrupts between a processor 310 and one or more SCSI devices 306. And the Gephardt et al. patent discloses an interrupt management of a multiprocessing system. The applied references do not teach or suggest a plurality of processors accessing a system bus that is arbitrated.

Even if combined as suggested by the Examiner, the references do not combine to teach or suggest a transceiver for use within a multi-tier system bus configuration including, among other claimed features, means for independently receiving instructions via the system bus from at least one of a plurality of processors and means for independently transmitting instructions via the system bus to at least one of the plurality of processors, wherein access to the multi-tier system bus is arbitrated.

For the foregoing reasons, Applicant's claims 1 and 9 are allowable. The remaining claims depend from independent claim 1 and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

All objections and rejections raised in the Office Action having been addressed, it is respectfully submitted that the application is in condition for allowance and a Notice of Allowance is respectfully solicited.

Respectfully submitted,

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